Listing of Claims

1. (Previously presented) An integrated circuit device comprising:

a core block configured for dynamic simulation testing and having an associated plurality of output ports, wherein the core block generates core output data for the plurality of output ports;

an input side sub logic circuit unit configured for dynamic simulation testing and coupled to a plurality of input ports of the core block that generates sub data for the plurality of input ports of the core block responsive to data input to the input side sub logic circuit unit; and

a multiplexer (MUX) unit between the core block and the input side sub logic circuit unit that selectively provides the sub data or the core output data as inputs to the input ports of the core block, without synchronizing therebetween, responsive to a MUX control signal,

wherein the core block generates the core output data for the plurality of output ports responsive to outputs from the MUX.

2. (Original) The integrated circuit device of Claim 1 further comprising an output side sub logic circuit unit configured for dynamic simulation testing and coupled to the plurality of output ports of the core block that outputs final output data responsive to the core output data from the core block.

3. (Original) The integrated circuit device of Claim 2 wherein the MUX unit comprises a plurality of multiplexers, ones of which are associated with respective ones of the input ports of the core block.

4. (Previously presented) An integrated circuit device comprising:

a core block having a plurality of output ports and a plurality of input ports and a vector input terminal, wherein the core block generates core internal data and wherein the core block is configured to output the core internal data during scan testing and to selectively

generate core output data for the output ports responsive to the core internal data or to test vector serial input data from the vector input terminal;

an input side sub logic circuit unit configured for dynamic simulation testing and coupled to the input ports of the core block that generates sub data for the plurality of input ports responsive to data input to the input side sub logic circuit unit; and a multiplexer (MUX) unit between the core block and the input side sub logic circuit unit that selectively provides the sub data or the core output data as inputs to the input ports of the core block, without synchronizing therebetween, responsive to a MUX control signal, wherein the core block generates the core internal data responsive to outputs from the MUX.

5. (Original) The integrated circuit device of Claim 4 further comprising an output side sub logic circuit unit configured for dynamic simulation testing and coupled to the plurality of output ports of the core block that outputs final output data responsive to the core output data from the core block.

6. (Original) The integrated circuit device of Claim 5 wherein the core block comprises:

a first core logic circuit unit that generates the core internal data; and

a scan test circuit unit coupled to the first core logic circuit unit and the vector input terminal that is configured to output the core internal data during scan testing and to selectively output data associated with ones of the output ports responsive to the core internal data or to the test vector serial input data.

7. (Original) The integrated circuit device of Claim 6 wherein the core block further comprises a second core logic circuit unit coupled to the scan test circuit that generates the core output data responsive to the output data associated with ones of the output ports received from the scan test circuit unit.

8. (Original) The integrated circuit device of Claim 7 wherein the scan test circuit

unit comprises a plurality of multiplexers and at least one flip-flop for each output port.

9. (Original) The integrated circuit device of Claim 8 wherein the scan test circuit unit consists of two multiplexers and one flip-flop for each output port.

10. (Original) The integrated circuit device of Claim 7 wherein the scan test circuit unit comprises at least one multiplexer and at least one flip-flop for each output port.

11. (Original) The integrated circuit device of Claim 10 wherein the scan test circuit unit consists of one multiplexer and one flip-flop for each output port.

12. (Original) The integrated circuit device of Claim 7 wherein the core block has a vector output terminal and wherein the scan test circuit unit is configured to serially output the core internal data to the vector output terminal during scan testing.

13. (Previously presented) A method for testing an integrated circuit device in which a plurality of associated macro blocks to be tested are configured for dynamic simulation testing, the method comprising:

generating at a first sub logic circuit unit of the macro blocks sub data for input to a plurality of input ports of a core block of the macro blocks responsive to data input to the first sub logic circuit unit core from external to the macro blocks;

providing the sub data and/or output data for a plurality of output ports of the core block to a multiplexer (MUX) unit coupled between the core block and the first sub logic circuit that selectively provides the sub data or the output data as inputs to the input ports of the core block, without synchronizing the output data between the output ports of the core block and the MUX unit, responsive to a MUX control signal; and

generating at the core block core output data for the output ports from the MUX input to the input ports of the core block.

14. (Previously presented) A method for testing an integrated circuit device in which a core block of a plurality of associated macro blocks to be tested has a vector input terminal and is configured for scan testing and others of the associated macro blocks are configured for dynamic simulation testing, the method comprising:

generating at a first sub logic circuit unit of the others of the associated macro blocks sub data for input to a plurality of input ports of the core block responsive to data input to the first sub logic circuit unit core from external to the macro blocks;

providing the sub data and/or output data for a plurality of output ports of the core block to a multiplexer (MUX) unit coupled between the core block and the first sub logic circuit that selectively provides the sub data or the output data as inputs to the input ports of the core block, without synchronizing the output data between the output ports of the core block and the MUX unit, responsive to a MUX control signal; and

generating at the core block core internal data responsive to the inputs to the input ports of the core block;

outputting from the core block the core internal data during scan testing; and

selectively generating at the core block core output data for the output ports responsive to the core internal data or to test vector serial input data from the vector input terminal.

15. (Previously presented) A semiconductor device comprising:

a first sub logic circuit unit which is designed to be adaptable for a dynamic simulation test method and generates sub data for each port by processing data received from the outside;

a MUX unit which is controlled by a MUX control signal and selectively outputs the sub data for each port or core output data for each port;

a core block which is designed to be adaptable for the dynamic simulation test method and generates the core output data for each port by processing the output data for each port received from the MUX unit, wherein the MUX unit selectively outputs the core output data for each port without synchronizing the core output data between the core block and the

MUX unit; and

a second sub logic circuit unit which is designed to be adaptable for the dynamic simulation test method and outputs final output data to the outside by processing the core output data for each port received from the core block.

16. (Previously presented) A semiconductor device comprising:

a first sub logic circuit unit which is designed to be adaptable for a dynamic simulation test method and generates sub data for each port by processing data received from the outside;

a MUX unit which is controlled by a MUX control signal and selectively outputs the sub data for each port or core output data for each port;

a core block which generates core internal data by processing the output data for each port received from the MUX unit and outputs the core internal data for each port to the outside by using a scan test method or generates the core output data for each port by selectively processing the core internal data for each port or serial input data for each port used as a test vector, wherein the MUX unit selectively outputs the core output data for each port without synchronizing the core output data between the core block and the MUX unit; and

a second sub logic circuit unit which is designed to be adaptable for the dynamic simulation test method and outputs final output data to the outside by processing the core output data for each port received from the core block.

17. (Original) The semiconductor device of Claim 16, wherein the core block comprising:

a first core logic circuit unit which generates the core internal data for each port by processing the output data for each port received from the MUX unit;

a scan test circuit unit which outputs the core internal data for each port to the outside by using the scan test method or selectively outputs the core internal data for each port or the serial input data for each port used as the test vector; and

a second core logic circuit unit which generates the core output data for each port by processing the output data for each port received from the scan test circuit unit.

18. (Original) The semiconductor device of Claim 17 wherein the scan test circuit unit comprises two MUXes and one flip-flop for each port.

19. (Original) The semiconductor device of Claim 17 wherein the scan test circuit unit comprises one MUX and one flip-flop for each port.

20. (Previously presented) A test method of a semiconductor device in which all macro blocks are designed to be adaptable for a dynamic simulation test method, the test method comprising:

generating sub data for each port by processing data received from the outside, at a first sub block included in the macro blocks;

selectively outputting the sub data for each port or core output data for each port, at a MUX included in the macro blocks and controlled by a MUX control signal, without synchronizing the core output data for each port between a core block included in the macro blocks and the MUX;

generating the core output data for each port by processing the output data for each port received from the MUX, at the core block included in the macro blocks; and

outputting final output data to the outside by processing the core output data for each port received from the core block, at a second sub block included in the macro blocks.

21. (Previously presented) A test method of a semiconductor device in which a core block of macro blocks is designed to be adaptable for a scan test method and other blocks of the macro blocks are designed to be adaptable for a dynamic simulation test method, the test method comprising:

generating sub data for each port by processing data received from outside, at a first sub block included in the other blocks of the macro blocks;

selectively outputting the sub data for each port or core output data for each port, at a MUX included in the other blocks of the macro blocks and controlled by a MUX control signal, without synchronizing the core output data for each port between the core block and the MUX;

generating core internal data for each port by processing the output data for each port received from the MUX or generating the core output data for each port by selectively processing the core internal data for each port or serial input data used as a test vector received from outside, at the core block included in the macro blocks; and

outputting final output data to the outside by processing the core output data for each port received from the core block, at a second sub block included in the other blocks of the macro blocks.

22. (Original) The test method of Claim 21 wherein the core internal data for each port can be outputted to the outside by a scan test circuit using the scan test method.

23. (Original) The test method of Claim 22 wherein the scan test circuit comprises two MUXes and one flip-flop for each port.

24. (Original) The test method of Claim 23 wherein the scan test circuit comprises one MUX and one flip-flop for each port.